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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 08/169,127
Filing Date: December 20, 1993
Appellant(s): SHINOHARA ET AL.

Mark W. Butler
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/17/2008 appealing from the Office action mailed 11/17/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is **substantially correct**, however the **objection** to informalities in claims 71-80, 93-49, 101 & 106-107 is not a rejection & is **not included** in this appeal, and the inclusion of claims 176-180 in the 112, first paragraph rejection have been withdrawn, which rejection thus properly reads:

Claims 61-65, 71-75, 91, 144, 151, 155-163, 166-167, & 173-175 are rejected under **35 U.S.C. 112, first** paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

Claims 176-180 are rejected under **35 U.S.C. 112, first** paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

6,261,856 B1	SHINOHARA et al.	07-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the **first paragraph of 35 U.S.C. 112**:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the **second paragraph of 35 U.S.C. 112**:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Appellants regards as his invention.

Claims 61-65, 71-75, 91, 144, 151, 155-163, 166-167 & 173-175 are rejected under **35 U.S.C. 112, second** paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellants regards as the invention.

Process claims, such as independent claims 61, recite formation of a non-single crystalline semiconductor layer and irradiation thereof, but then require "removing an insulating layer

comprising silicon oxide from an upper surface of the crystallize semiconductor layer", however it is unclear from the claim language where this silicon oxide layer comes from, since it was never claimed to be deposited, hence it is unclear how one can remove something that does not necessarily exist. It also leaves the claim open to speculation, since this insulating layer was not necessarily present when irradiation occurred, did the irradiation while crystallizing the semiconductor layer, also cause surface oxidation, or was it deposited before, thus affecting the irradiation process, etc? Also, lacking any knowledge of where on the upper surface this insulating layer resides, it could be a masking layer (e.g. all laser irradiation is not transparent to silicon oxide), such that irradiation is blocked from some areas of the semiconductor layer, but not others, using a lateral crystallization technique. Also, where is Appellants' support for a silicon oxide layer that has no clear origin? Pages 11-12 indicate that an insulating layer (silicon oxide or silicon nitride having thickness 200-1500 Angstroms) that has been deposited on a semiconductor layer, then patterned to form semiconductor islands (semiconductor plus insulating layer), which are irradiated, then the insulating layer is removed after crystallization & a different insulating layer then deposit thereon, but due to the uncertainty in the claim language, the scope of the claim is not limited to such a situation.

It is noted that claims 176-180 can be considered to essentially correct the clarity problem by supplying clearer context (and partial support as discussed below).

Claims 61-65, 71-75, 91, 144, 151, 155-163, 166-167, & 173-175 are rejected under **35 U.S.C. 112, first** paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As noted above in the discussion with respect to the 112, second paragraph, the scope of the claims is inclusive of options that are broader than the scope of the enabling disclosure (e.g. lacking with respect to their relationship of where they reside during the crystallization, etc.), hence will encompass options not supported by the more specific disclosure of the specification, thus encompass New Matter.

Note, claims 176-180 have been removed from this rejection, since on re-review, as pointed out by appellants, the preceding claims identified location of the silicon oxide as on "an upper surface of the crystallized semiconductor layer", therefore in claims 176-180 where the insulating layer comprising silicon oxide is required to form before the claimed irradiating, does sufficiently clearly necessitate a location, when these dependent claims are properly combined with the preceding claims.

Claims 61-65, 71-75 are rejected under **35 U.S.C. 112, first** paragraph, because the specification, while being **enabling for** an insulating layer of silicon oxide or silicon nitride having a thickness of 200-1500 Angstroms deposited before the irradiation step, where the irradiation crystallization process is performed with the insulating layer covering the semiconductor layer being crystallized, and where this insulating layer is removed (etched) after irradiation before proceeding with further processing steps, does **not reasonably provide enablement for** removal of "an insulating layer comprising silicon oxide" from an unknown source in an uncertain relationship to the irradiation step itself. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

See above discussion.

The **nonstatutory double patenting rejection** is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would

have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 61-80, 91-94, 101, 104-107, 131 & 140-175 are rejected under the judicially created doctrine of **obviousness-type double patenting** as being unpatentable over **claims 1-39** of U.S. Patent No. **6,261,856 B1**.

Although the conflicting claims are not identical, they are not patentably distinct from each other, because the claims of the patent to Shinohara et al (856) were found to contain limitations of the crystallization process claims, where limitations are claimed in different orders, such as in some patented independent claims, the semiconductor is generic & in some it is amorphous Si or solid phase crystallized silicon or comprises crystallized silicon. The present claims have been broadened from amorphous silicon into non-single crystalline semiconductor layer, which encompasses & overlapped with the patented claims' semiconductor film or amorphous silicon or comprising crystallized silicon, especially considering that since the layer in the patent claims may or may not be initially crystallized or amorphous, thus are obvious variations of overlapping scope. It was noted that the insulating (Si Oxide & Si Nitride) layers (patent claims 1, 6, 17 & 24) in the patent may be called "blocking layers" (claims 27-28 & 33-34) without "ion" being explicitly stated, but the ion blocking function is inherent or obvious by context of like configurational placement of like compositions in the claimed "active matrix circuit and driving circuit", so is considered equivalently used in the patent claims, especially considering that the patent derives its support for its terms' meaning from the same disclosure as the present case. The

semiconductor film thickness of 200-1500 angstroms is in patent claim 8, but has been deleted from the present claims, hence is no longer an issue. Appellants have previously amended claim 61 & analogous claims 71, 144, 155 & 168 (see above), to add the limitation of removing a layer, which is not necessarily even there, hence as presently written this limitation cannot effect clear differentiation (see clarity discussion above), as there may be nothing to remove or it is unclear how to remove a layer which may not be present.

Claims 66 and analogous claims have been amended to include the non-single crystal semiconductor layer having been doped with boron or arsenic, & modified the moving limitation, however the patent claims have limitations to moving, which are not significantly differentiated by adding the phrasing of "a relative location", and they also include use of dopant impurities, such as boron and arsenic, as exemplified by patent claim 26, thus these limitations added to the claims do not provide significant differentiation, thus do not remove the obviousness double patenting rejections.

Also note with respect to forming a insulating layer on the semiconductor layer and thereafter irradiating (e.g. present claim 140 or 141), that claim 27 of the patent include such a process of forming claimed active-matrix circuit & driving circuit devices, formed on semiconductor islands of crystallized silicon, which read on the claimed "non-single crystalline semiconductor layer" or "solid phase crystallized silicon". Also see claim 33. Furthermore, while the patent claims do not specify deposition of metal gate electrodes (as exemplified in present independent claim 141), they are claiming formation of thin film transistors, with active matrix circuit and driving circuit, hence in order to be functional they must have deposition of such electrodes in order to complete the device formation, where metal is a conventional material used therefore, & the patented claims do discuss gate electrodes used as masks (claims 27 or 33), hence it would've been obvious to one of ordinary skill in the art in order to perform the complete formation of claimed device formation processes via the use of metal for the gate electrodes &/or to perform this additional step, thus the claims are seen as obvious variations on the present claims.

(10) Response to Argument

With respect to the **112, second** paragraph rejection, in Appellants' arguments, it appears to be their position that as long as the specification discusses a specific layer, that they do not have to clearly claim the deposition of that layer when discussing a deposition sequence and treatment of other deposited layers, in order to remove that previously non-claimed layer. However, the examiner does not agree, as in semiconductor processing, there are many uses for insulating layers & many sources & uses of silicon dioxide, especially when one of the layers involved happens to be silicon (e.g. specific elemental species of the semiconductor layer), thus failing to clearly specify the origin & location of a layer to be removed, creates numerous questions of scope & clarity as discussed above. The fact that the specification discloses & supports deposition of the insulating layer in a specific location in a specific deposition sequence, does not mean that the claims must be read to deposit this layer, if deposition of it is never claimed, just the removal of the a silicon oxide insulating layer, which may or may not be what was discussed in the specification, i.e. the specification does not define all insulating layers comprising silicon oxide to be to be the specific layer in the specific position of the particular example in the specification, so it would not be proper to read the claims, as written, as if such was the only option.

Furthermore, on page 18 of appellants' Brief, they discuss insulating layer 53 as shown in figure 7(c) as the exemplary support, however as can be seen from figures 7(a-b), & the discussion on page 10-11, the semiconductor layer was crystallized as illustrated in figure 7(b), before deposition of insulating layer 53, with page 12, lines 1-2 etching off insulator 59 after crystallization, then depositing insulating layer 53 by sputtering. Note insulating layer 59 illustrated in figure 7(a-b) may have relevance, but appellants' own confusion of different insulating layers in citing their support, illustrates the necessity of clarity in the claims. Also note that appellants' inference on page 18 of the 11 /17 /2008 Brief that insulating layer 53 is an oxide layer requiring removal, would indicate that for gate insulating layer of

claims 27 & 33 of copending 6,261,586 "one of ordinary skill in the art would readily appreciate... an oxide layer requiring removal" also, as its teachings come from the same disclosure, such that considering this argument of appellants, would argue for including claims 176-180 in the obviousness double patenting rejection! However, the examiner did not note a suggestion in the copending claims or pages 12-13 of the present specification to remove insulating layer 53/gate electrode, and thus despite appellants' arguments, such in conclusion would be inappropriate.

Appellants request in their remarks on the top of page 19 in their 11/17/2008 Appeal Brief to remove claims 176-180 from the 112 second rejection is not understood, as these claims have never been part of this rejection, as was apparently previously recognized by appellants in their statement of the grounds & previous restatement at the beginning of the argument section.

With respect to the **112, first** paragraph rejections, the majority of appellants' arguments appear to be directed to claims 176-180, where as noted above appellants' arguments with respect to these five dependent claims has been essentially agreed with, thus if properly combined with their independent claims or claims 178+144 or claims 180+167 would need to be combined (also possibly with their with independent claims 66 or 76, respectively). Appellants' arguments do not appear to refute the lack of support, thus enablement, except when properly combined with claims 176-180.

With respect to the **obviousness double patenting rejection**, on page 22 in their arguments, it appears that appellants are basing their differentiation of the patent claims from present claims 61, 71 & 151 on unclaimed requirements (i.e. the silicon oxide insulating layer that is never necessarily deposited), where the patent claims are derived from essentially the same specification as the present claims derive their limitations. The examiner fails to follow appellants' logic of selectively reading unclaimed limitations into the claims to differentiate claims both based on the same specification.

With **respect to claims 66, 76 & 152**, appellants' discussion on page 22 of their brief fails to explain how their presently claimed limitation of "moving a relative location of said substrate to the

condensed laser beam along a third direction orthogonal to the first direction" somehow significantly differentiates from analogous limitations in the copending patent's claims, such as in claim 12's "moving said substrate with respect to said laser beam in a direction perpendicular to the first direction..." (where both first directions are describing like expanding steps, a relative location encompasses "moving... with respect to...", & orthogonal is a synonym of perpendicular). Also note that "third direction" is not necessarily different than "second direction" present in both sets of claims, especially as the specification does not appear to encompass moving the substrate up and down!

With **respect to claims 140, 153 & 164**, which have been noted to relate to claims 27-28 & 33-34 in copending patent (856) , appellants in the paragraph bridging pages 22-23, have failed to explain how their present "ion blocking film", which may be silicon oxide or silicon nitride, is somehow different than the patented "blocking film" which may also be the same materials, where both claims have semiconductor islands formed thereon, followed by gate insulating films, gate electrodes & laser treatment, all derived from the same specification examples, so how could these overlapping process steps contain some particularly critical difference, since the patented claims gate insulating electrode is not excluded from deposition on any exposed surfaces of the [ion] blocking film, nor read in light of the specification would one of ordinary skill in the art reasonably exclude deposition thereon, especially considering that "forming a gate insulating film on said plurality of semiconductor islands" would appear to indicate that a single blanket gate insulating film is formed over all the islands, thus expected to also cover intervening space between, i.e. exposed blocking between islands.

With **respect to claims 71, 76, 164 & 165**, appellants cite the limitation of "forming a plurality of thin film transistor is... for the active-matrix circuit and said peripheral circuit [for driving pixel TFTs] "as differentiating from copending (856), however the copending patent's claims are also directed to "... active-matrix circuit and driving circuit are constituted with said thin film transistors" (claim 1 of (856)), but the difference of the word "peripheral" when added into the description of apparently otherwise

identical driving circuits & with no discussion of driving circuits, peripheral or not, in appellants' citations on pages 1 or 2 or 3, which are alleged to demonstrate these claims' significance with respect to the patented claims derived from the same disclosure, thus these cited disclosures cannot be considered to provide any criticality to the description of "peripheral", describing "a peripheral circuit for driving pixel TFTs. Also note, in the present specification on page 12, lines 22-23, the disclosure for the active matrix circuit devices has no mention of peripheral, but page 11, lines 6-11 disclose "The islands are arranged in rows and columns as shown in Fig. 8. For clarification, only 5 x 5 islands are shown in Fig. 8. ... It is also possible to form other semiconductor islands on the same surface in order to form a driver circuit or peripheral circuit for driving the pixel TFTs", which could indicate that a driver circuit is the same as or that it is equivalent to a peripheral circuit for driving, such that there cannot be considered a significant difference between the presently claimed term using "peripheral" in the claim language in Shinohara et al. (856). Thus, while appellants' state in their last full sentence on page 23 of the 11/17/08 brief that support for the term "peripheral circuit" is found in figures 5A, 5B and 8, the actual disclosure on page 11, describing figure 8 appears to say that figure 8 does not show peripheral circuits & that for peripheral circuits are merely another equivalent alternative to the particular "island" arrangement shown, without defining what peripheral circuits are (unless they are driver circuits), nor any criticality in their use. With respect to figures 5 (A&B), what support these micrographs of a groove in an ITO film described on page 9, lines 9-25 might provide to the discussion on "peripheral" with respect to circuits is completely unapparent.

Appellants have for the first time in this 11/17/2008 Appeal Brief cited US patents 7,381,599 B2 (Konuma et al.) & 7,416,907 B2 (Yamazaki et al.) for providing evidence that one of ordinary skill in the art would regarding "peripheral circuit" as an art recognized. While the citations do the use that term "peripheral circuits" (Yamazaki et al. (907)) or phrasing such as "driver TFTs in peripheral circuit" (Konuma et al.), they provide no definition of the term claimed, nor provided any

apparent meaning that would significantly differentiate the claimed "peripheral circuit for driving pixel TFTs" from the patented claim limitation of "said active matrix circuit and said driving circuit are constituted with said thin film transistors", as it is not apparent from appellants' specification or the cited references that the use of the adjective "peripheral" provide any significant meaning to the description of the circuit being formed, or that if the patented claims are considered to be directed to the generic, that the specific claim of "peripheral circuit..." would not have been reasonably expected by one of ordinary skill in the art to be an expected option.

With **respect to claims 141 & 154**, on page 22 of their Brief appellants recite a limitation concerning condensing the laser cross-section, which is analogous to similar limitations in the other of their independent claims not included in this argument, and present in the patent's independent claims, as discussed in the above rejection, it is unclear why appellants discuss these two claims separately from the rest of the claims, nor what Shinohara et al. (856)'s alleged recitation of a wavelength of the laser beam, supposedly exemplified by their claim 2, has to do with the alleged inappropriateness of the obviousness double patenting rejection, especially given that (856)'s claim 2 is directed to further defining the type of device formed, not a wavelength used.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Marianne L. Padgett/

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